The Voltage-Dependent IP3 Performance of a 35-GHz InAlAs/InGaAs-InP HBT Amplifier

K. W. Kobayashi, A. K. Oki, J. Cowles, L. T. Tran, P. C. Grossman, T. R. Block, and D. C. Streit

***Abstract*—Here we report on the first IP3 results of a 35-GHz Ka-band amplifier based on InAlAs/InGaAs-InP heterojunction bipolar transistors (HBT's). The amplifier combines four 1×10 μm^2 Quad-emitter HBT devices for a total emitter area of 160 μm^2 to achieve a gain of 5 dB and an IP3 of 26.5 dBm at 35 GHz. IP3 was characterized over collector bias voltage and indicates that there is an optimum V_{ce} corresponding to a maximum IP3 to dc power ratio, which is related to the HBT nonlinear voltage-dependent collector-base capacitance. A maximum IP3-to-dc power linearity figure of merit (LFOM) of 4.1 is achieved at a total collector current of 48 mA and a low V_{ce} of 2.25 V. This LFOM is comparable to HEMT's at these frequencies and is expected to improve with the maturity of InAlAs/InGaAs-InP HBT technology.**

***Index Terms*—Amplifier, HBT, InP, IP3.**

I. Introduction

HETEROJUNCTION bipolar transistors (HBT's) have been regarded as a potential technology for high-IP3 amplifiers used in wide dynamic range receivers. Previous work has demonstrated AlGaAs/GaAs HBT devices with phenomenal IP3-to-dc power ratios of ≈44 at 12 GHz, which is a factor of 7–10 better than conventional MESFET and HEMT devices at these frequencies [1]. These results indicate that high linearity is achieved from HBT devices inspite of their highly nonlinear base-emitter diode I–V characteristics. A study of the HBT two-tone IM3 characteristics has suggested that the high linearity performance is strongly dependent on the base and emitter device resistances, which provide negative feedback, as well as the voltage modulation immunity of the collector-base capacitance as the collector goes through its output voltage excursion along a given load-line [2]. The nonlinear characteristics of the HBT C_{cb} capacitance is heavily dependent on the HBT's collector epitaxy structure. III–V-based HBT's inherently possess an advantage in voltage immunity C_{cb} characteristics, which can result in less output distortion and higher IP3 performance. The rationale behind this statement is that the fundamentally higher electron mobility attained in GaAs and InP-based HBT's allows very low HBT collector doping concentrations to be employed without incurring device performance penalties due to the "base pushout" effects commonly observed in silicon bipolar junction transistors (BJT's). The lightly doped collector region of the HBT's can provide a very linear fixed C_{cb} capacitance at a low voltage bias in a region where the collector is fully depleted of carriers. In this low voltage reverse bias region, the collector-base junction behaves like a reversed-biased p-i-n diode whose microwave linearity characteristics improve the output linearity of the HBT device. In fact, IP3's as high as +35 dBm have been demonstrated for an X-band single-pole two-throw p-i-n diode switch fabricated from the inherent collector-base junction of a GaAs HBT device [3].

Previously, high-IP3 performance of a 5–11 GHz AlGaAs/GaAs HBT high intercept amplifier has been reported that achieves IP3's exceeding 32 dBm and a LFOM of 13.5 [4]. More recently, a millimeter-wave frequency Q-band AlGaAs/GaAs HBT balanced amplifier was reported that obtains a LFOM of 3–3.7 at 35 GHz and a record LFOM of 11.6 at 44 GHz [5]. This Q-band work demonstrates the feasibility of HBT's for high-IP3 amplifier applications at millimeter-wave frequencies. Upcoming InP-based HBT's possessing higher intrinsic electron mobility can offer higher frequency capability, but these have been relatively unexplored for millimeter-wave amplifier applications. In this work, we report on the first IP3 characteristics of a Ka-band InAlAs/InGaAs-InP-based HBT amplifier that demonstrates comparable IP3 performance at 35 GHz and indicates strong promise for high linearity front-end applications in the millimeter-wave range. In addition, a discussion on the voltage-dependent (V_{ce}) IP3 characteristics of the amplifier is provided, as well as suggested modifications that can be made to the HBT device in order to achieve higher IP3 performance per dc power.

II. InAlAs/InGaAs-InP HBT Technology

The Ka-band amplifier was fabricated using InAlAs/InGaAs-InP HBT device MBE technology. The InAlAs/InGaAs HBT device structure is grown by molecular beam epitaxy (MBE) on a semi-insulating 2-in InP substrate. Be and Si are used as p- and n-type dopants for the base and emitter/collector, respectively. The emitter incorporates an 800-Å InGaAs cap, which is highly doped to obtain low emitter contact resistance. The intrinsic emitter region is 1200 Å thick and doped to 5×10^{17} cm^{-3}. The base-emitter junction is compositionally graded from InGaAs to InAlAs to form HBT's with very repeatable beta and low V_{be} characteristics. The base-collector epitaxial structure consists of a base thickness of 800 Å uniformly doped to 3×10^{19} cm^{-3}, a 7000-Å-thick n-type collector lightly doped to 1×10^{16} cm^{-3}, and an N^+ sub-collector doped to 1×10^{19} cm^{-3}. The HBT dc beta across the wafers are typically >20

Manuscript received September 23, 1996.

The authors are with TRW Electronics Systems and Technology Division, Redondo Beach, CA 90278 USA.

Publisher Item Identifier S 1051-8207(97)01773-X.

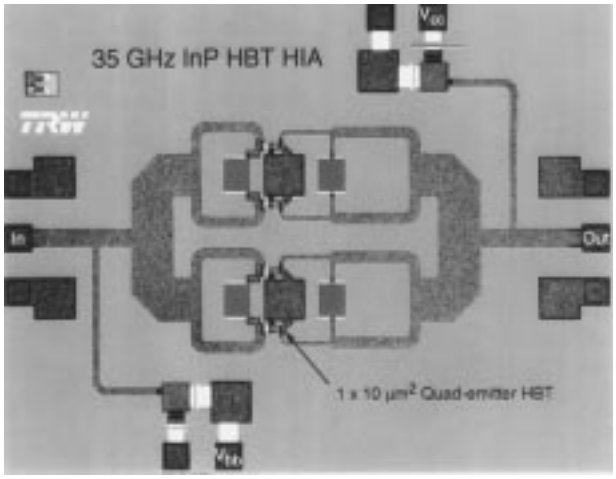

Fig. 1. Microphotograph of the 35-GHz Ka-band HBT amplifier. Chip size is 2.4 × 1.8 mm^2.

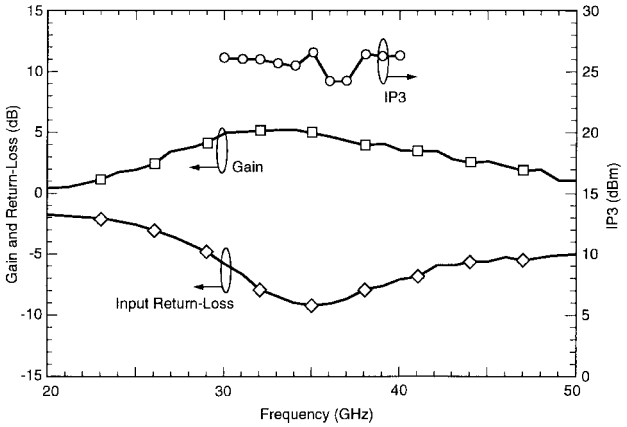

Fig. 2. Broadband Gain, IP3, and input return-loss response of the HBT amplifier at a total $I_{ce} = 48$ mA and a $V_{ce} = 2.25$ V.

at a current density of $J_c = 40$ kA/cm^2. The breakdown voltage BV_{ceo} is ≈8 V and the BV_{cbo} is ≈ 13 V.

A fully self-aligned HBT process is used to produce 1-μm emitter width HBT's and which features a new HBT base-undercut profile for reducing the collector-base capacitance and improving the device f_T and f_{max} performance. The 1-μm emitter width HBT devices have achieved peak f_T's and f_{max}'s of 80 and 200 GHz (from unilateral gain), respectively. These numbers were obtained from a 1 × 10 μm^2 quad-emitter HBT's biased at a current density of $J_c \approx$ 50–60 kA/cm^2 and a $V_{ce} = 2.0$ V and is the same device cell used in the amplifier design of this work.

III. Ka-Band InAlAs/InGaAs-InP HBT Amplifier Design and Results

Fig. 1 shows a microphotograph of the 35-GHz Ka-band HBT amplifier. The amplifier combines four 1 × 10 μm^2 Quad-emitter HBT devices, which comprise a total emitter area of 160 μm^2. Each of the four transistors are prematched to an intermediate real impedance and then four-way combined to 50 Ω at both the input and the output. Shorted quarter-wave transmission lines comprise the base and collector dc bias networks. Each of the four HBT devices is biased at an $I_{ce} = 12$ mA. The total monolithic microwave integrated circuit (MMIC) is 2.4 × 1.8 mm^2 in area.

Fig. 2 gives the broadband gain, IP3, and input return-loss response of the HBT amplifier at a total $I_{ce} = 48$ mA and a $V_{ce} = 2.25$ V. A gain of 5 dB was obtained at 35 GHz. The input return-loss is >12 dB at this frequency. The IP3 varies from 24–26.5 dBm and is reasonably flat across a 30–40-GHz band with a peak IP3 of 26.5 dBm at 35 GHz.

The IP3 was also characterized at 35 GHz and a nominal current of 48 mA as a function of V_{ce} bias voltages. Fig. 3 gives both the IP3 and calculated linearity figure of merit ratio defined by IP3 (in milliwatts)/dc power (milliwatts). This figure shows that as the V_{ce} voltage is increased, the IP3 also increases. At a V_{ce} voltage of ≈2.25 V, the amplifier achieves a maximum IP3 of 26.5 dBm while consuming only 106 mW of dc power. For higher voltages, the IP3 levels off. A plot of

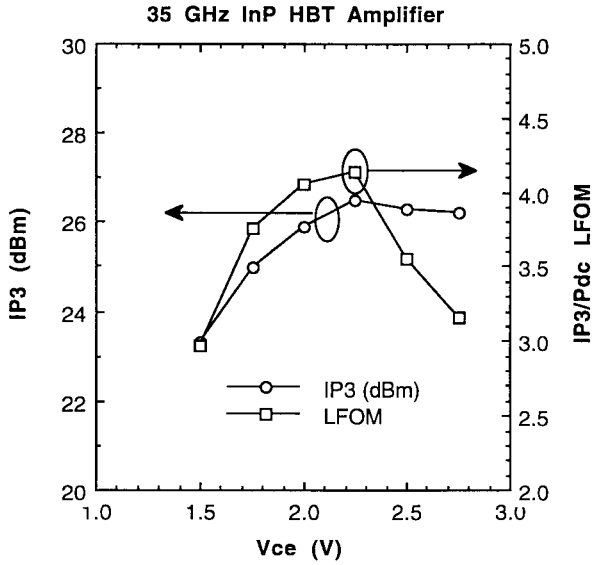

Fig. 3. IP3 and calculated LFOM ratio defined by IP3 (in milliwatts)/dc power (milliwatts).

the IP3/P_{dc} LFOM ratio illustrates a peak ratio of 4.1 at a V_{ce} of about 2.25 V. The IP3 data of Fig. 2 suggests that there is a V_{ce} voltage above which IP3 does not significantly improve, and that a maximum IP3/P_{dc} ratio occurs around this voltage.

The voltage-dependent IP3 performance is believed to be heavily related to the nonlinear collector-base capacitance characteristics as suggested in [2]. This nonlinear C_{cb} characteristic is illustrated in Fig. 4, which shows the C_{cb} capacitance as a function of HBT V_{ce} voltage. The collector-base capacitance characteristic was derived from S-parameters as well as physical calculations of the C_{cb} capacitance for a 1 × 10 μm^2 Quad-emitter HBT device. The voltage-dependent C_{cb} characteristic is comprised of a combination of piece-wise linear and nonlinear functions. At low V_{ce} bias, the collector-base junction can be modeled by the following nonlinear relation:

$$C_{jc} = \frac{C_{jo}}{\left(1 + \frac{V_{ce} - V_{bc}}{V_{jc}}\right)^m} \quad (1)$$

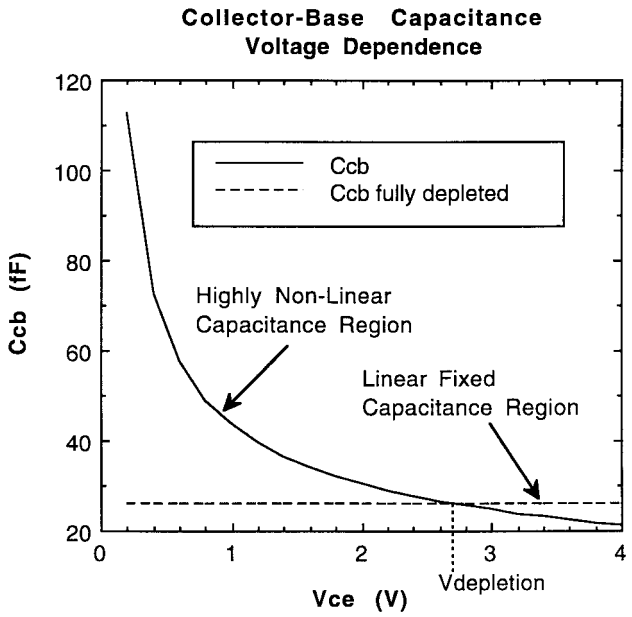

Fig. 4. Collector-base capacitance versus V_{ce} for a 1 × 10 μm^2 Quad-emitter HBT.

where the zero-bias base-collector junction C_{jo} is 50 fF, the junction potential $V_{jc} = 0.74$ V, the base-emitter turn-on voltage $V_{be} \approx 0.8$ V, and the exponent m characterizing an abrupt collector-base junction is 0.5. As the V_{ce} voltage is increased, the collector-base junction becomes fully depleted and is characterized by a fixed linear capacitance. Thus, as the voltage is increased, the C_{cb} capacitance approaches a more linear capacitance region where high amplifier IP3 is observed (see Fig. 3). As one reaches a voltage where full depletion occurs, the IP3 is expected to level off, as indicated by Fig. 3. The onset where full depletion occurs is demarked by a voltage $V_{depletion}$, where the two piece-wise capacitance functions intersect. The $V_{depletion}$ for these InP-based HBT's is approximately 2.7 V, as indicated by Fig. 4, which is slightly higher than is suggested by the amplifier IP3 performance of Fig 3. In order to achieve maximum IP3 per dc power LFOM, $V_{depletion}$, where the onset of full depletion occurs can be lowered, which reduces the operating voltage and dc power consumption at maximum IP3. This can be achieved by either reducing the thickness of the n^- type collector region, which moves up the fixed full-depleted capacitance asymptote of Fig. 4, or by reducing the n^- type collector doping from 1 × 10^{16} cm^{-3} down to 5 × 10^{15} cm^{-3} (≈ intrinsic background doping), which creates a wider collector depletion region for a given voltage. Employing both modifications will lower the V_{ce} voltage required to achieve a given IP3 and should result in higher HBT IP3 performance under lower power operation without significantly impacting the gain response. Further experimental investigation is underway to verify these ideas.

IV. Conclusion

The first IP3 results of a 35-GHz Ka-band amplifier based on InAlAs/InGaAs-InP HBT's has been reported. The amplifier achieves a gain of 5 dB and an output IP3 of 26.5 dBm at 35 GHz while consuming only 106 mW of dc power. A maximum IP3-to-dc power LFOM of 4.1 is achieved at a total collector current of 48 mA and a low V_{ce} of 2.25 V. IP3 voltage-dependent characteristics have been related to the voltage-dependent nonlinear HBT collector-base capacitance. Suggestions on how the HBT collector epitaxy structure can be redesigned to improve the C_{cb} linearity characteristics at lower operating voltages has been given, which is expected to result in higher IP3 performance per dc power consumption for the InAlAs/InGaAs-InP HBT's.

References

[1] M. E. Kim, A. K. Oki, G. M. Gorman, D. K. Umemoto, and J. B. Camou, "GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave applications," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1286–1303, Sept. 1989.

[2] N.-L. Wang, W. J. Ho, and J. A. Higgins, "AlGaAs/GaAs HBT linearity characteristics," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1845–1850, Oct. 1994.

[3] K. W. Kobayashi, A. K. Oki, D. K. Umemoto, S. K. Z. Claxton, and D. C. Streit, "Monolithic GaAs HBT *p-i-n* diode variable gain amplifiers, attenuators, and switches," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 2295–2302, Dec. 1993.

[4] B. L. Nelson, D. K. Umemoto, C. B. Perry, R. Dixit, B. R. Allen, M. E. Kim, and A. K. Oki, "High-linearity, low dc power monolithic GaAs HBT broadband amplifiers to 11 GHz," in *IEEE MMWMC-Symp. Dig.*, Dallas, TX, May 1990, pp. 15–18.

[5] Y. Kwon, W-J. Ho, and J. A. Higgins, "A Q-band monolithic linear amplifier using AlGaAs/GaAs HBT's," *IEEE Microwave Guided Wave Lett.*, vol. 6, pp. 180–182, Apr. 1996.